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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,542	09/30/2003	Moo Jin Lee	049128-5127	1841

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,542	LEE ET AL.	
	Examiner	Art Unit	
	Alexander Eisen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 5-6 and 18-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Nanno et al., (Nanno), WO02/35507 (patent family member-equivalent US 6,909,413 B2 is cited hereinafter for convenience).

With respect to claim 5 Nanno discloses a method for supplying a power for a liquid crystal display, comprising the steps of taking a power source voltage less than 3.0V from a system (1.8 V from a battery 12 in FIG. 1); supplying the power source voltage to the digital circuit devices including an interface circuit (power supply 24), a timing circuit (start pulse circuits and transfer clock circuits embedded into data and gate drivers, col. 7, lines 40-54, including terminals 21a-b and 22a-b, constitute timing circuit), a data driving circuit 22 and a gate driving circuit 21 for processing digital signal (to a circuitry for driving LCD (FIG. 2, 4; col. 7, ll. 5-39; col. 8, line 48 – col. 9, line 28).

As pertaining to claim 6, the method further comprises the steps of raising or reducing the power source voltage from the system to generate voltage to be supplied to the liquid crystal panel (FIG. 4).

As pertaining to claim 18, Nanno discloses an apparatus for supplying a power of a liquid crystal display comprising a system for generating a power voltage under 3.0V (battery 12

supplies 1.8 V); and at least one of digital circuit devices (LCD driving circuitry in FIG. 2) including an interface circuit (level shifter 25 and power supply 24), a timing circuit (start pulse circuits and transfer clock circuits embedded into data and gate drivers, col. 7, lines 40-54, including terminals 21a-b and 22a-b, constitute timing circuit), a data driving circuit 22 and a gate driving circuit 21used to process the digital signal while taking the power voltage.

As pertaining to claim 19, the apparatus further comprises a DC-DC converter (charge pumps CP1-CP3 in FIG. 4) for raising or reducing the power source voltage to generate the raise or the reduced voltage to be supplied to the liquid crystal panel.

As pertaining to claim 20, the digital circuit devices include an interface circuit for receiving a synchronous signal (FIGS. 11-12), a clock signal CL1, CL2 and digital video data (FIG. 12) from the system; a data driving circuit for supplying the digital video data to the liquid crystal panel (source driver circuit 22A in FIG. 9); a gate driving circuit (21 in FIG. 9) for supplying a scan pulse to the liquid crystal panel; and a timing controller (inherently present by the signal produced by timing controller) for controlling the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 7-11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owaku et al., JP 10-232652 (hereinafter Owaku) in view of Isozaki.

With respect to claim 1 and 7 Owaku discloses a method for supplying a power to a liquid crystal display, comprising the step of supplying a power source voltage from a system to digital circuit devices for processing digital signal (3.3 V is supplied from the system 10 to a display section 20 in FIG. 1; paragraphs [0020-21].

While Owaku discloses that the step of supplying 3.3 V to the display section is followed by the step of generating various voltages for supplying the display, Owaku does not disclose specifically the step of reducing the power source voltage from the system.

Isozaki teaches a liquid crystal display driving circuit which is using a lower voltage of 2.7 V for feeding the driving circuit in order to reducing power consumption of the circuitry (see FIGS. 1-2 and relevant description in col. 8-9).

It would have been obvious to one of ordinary skill in the art at the time when the invention was made to use the circuit provided by Isozaki in the system of Owaku, because such combination would help to reduce the power consumption by the LCD driving circuitry, and for such use the voltage from the system needs to be reduced to 2.7 V from the system voltage 3.3V to satisfy the power requirements of the circuit, which would be readily understood by those artisans and well within their skills to achieve.

As pertaining to claim 2, the power source voltage from the system is over 3.0V (3.3V as has been shown above).

As pertaining to claim 3, the reduced power voltage is under 3.0V (i.e. 2.7V).

As pertaining to claim 4,the method further comprises the step of raising or reducing the power source voltage from the system to generate voltage to be supplied to the liquid crystal panel (paragraph [0022] in Owaku and FIGS. 8-9 in Isozaki).

Claims 7-10 are apparatus claims corresponding to the method claims 1-4 and therefore are rejected on the same rationale: the combination Owaku-Isozaki teaches all the elements of the claims including DC-DC converter that generates required voltages.

As pertaining to claim 11, the digital circuit device comprises an interface circuit for receiving a synchronous signal (CEI/O), a clock signal (XSCL) and digital video data (Do~Dn) from the system; a data driving circuit (113 in FIG. 1 of Isozaki and 130 in FIG. 8 of Owaku) for supplying the digital video data to the liquid crystal panel; a gate driving circuit (140 in Owaku) for supplying a scan pulse to the liquid crystal panel; and a timing controller (104 in FIG. 1 of Isozaki) for controlling the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit.

As pertaining to claims 13-17, various circuits for reducing power supply voltage, such as pulse width modulator type, pulse frequency modulator type, a regulator for reducing the power source voltage from the system based on the comparison of the predetermined reference voltage and the output voltage, resistive (FIG. 21 in Nanno is an example) or RC integrating circuits are well known in the art, and therefore it would have been obvious to one of ordinary skill in the art at the time when the invention was made to use any of these voltage reducers in the display driver circuits of Owaku-Isozaki as an alternative choices without bringing about unexpected result or undue experimentation.

5. Claims 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owaku in view of Isozaki and further in view of Ishiyama, US 2003/0053321 A1.

Owaku and Isozaki teach all the limitations of claims 12 and 21 except a gamma reference voltage generated by voltage-dividing the VDD voltage,

Ishiyama teaches a gamma reference voltage generated by voltage-dividing the VDD voltage (see FIG. 7, paragraphs [0209-0212].

It would have been obvious to one of ordinary skill in the art at the time when the invention was made to add the gamma correction circuit to the driving circuit of Isozaki-Owaku, because it would improve the color displaying by the former, and that it could be implemented by any known method, using a voltage dividing by a resistor chain as taught by Ishiyama.

Response to Arguments

6. Applicant's arguments filed 20 September 2006 have been fully considered but they are not persuasive. The Applicant argues that the reference of record, Isozaki "fails to discloses both "reducing a power source voltage from a system" and "supplying the reduced power source voltage to digital circuit devices for processing digital signal". The examiner respectfully disagrees. Owaku teaches supplying a power source voltage 3.3V to a display processing circuitry 20 from the system 10, and Isozaki teaches that such circuitry may include components that require lower operating voltage, for example 2.7V. To provide such reduced voltage the voltage supplied from the system needs to be reduced (i.e. 3.3V supplied from the system in Owaku in order to feed components of the system requiring 2.7V voltage supply needs to be reduced by any known in the art methods). The rejection is maintained.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander Eisen
Primary Examiner
Art Unit 2629

8 December 2006